In the Specification

Please amend the specification of this application as follows:

Rewrite paragraph [0019] as follows:

--[0019] Referring now to Figure 1, a system 100 is shown in accordance with a preferred embodiment of the invention. As shown, the system 100 includes a memory unit 102 for storing data and a processor 104 for executing applications. In addition, system 100 includes a peripheral 106 coupled to a DMA controller 108. The peripheral 106 may transfer data to the memory 102 through, or otherwise by the action of, the DMA controller 108. In addition, data may be transferred from the memory 102 to the peripheral 106 though the DMA controller 108. The peripheral ~~104~~ 106 may include a hard drive, a tape backup, or other hardware unit that supports DMA transfers.--

Rewrite paragraph [0023] as follows:

--[0023] To perform a DMA transfer, the instantiated algorithm 206 preferably requests a logical channel from the DMA manager 214 through the DMA interface 210. The DMA manager 214 may receive the request and identify a suitable physical channel for the DMA transfer by interacting with the DMA controller ~~104~~ 108. After identification of a physical channel, the DMA manager 214 preferably grants a "handle" to the identified logical channel. The instantiated algorithm 206 receives the handle and may schedule a transfer using the handle. The handle may comprise a pointer to the logical channel that uniquely identifies the logical channel for the instantiated algorithm 206.--

Rewrite paragraph [0026] as follows:

--[0026] Referring to Figure 4, a diagram of an exemplary DMA mechanism is shown. To schedule a DMA transfer, a set of control

registers 400 accessible to the DMA controller ~~104~~ 108 preferably are written to by the DMA manager 214 (Figure 2). Within the control registers 400 exist one or more trigger registers 402 that trigger the DMA controller ~~104~~ 108 to place the transfer into a hardware queue 404. The transfer preferably is placed into a hardware queue 404 after a trigger register 402 is written to by the DMA manager 214. While in the queue 404, the transfer waits, if necessary, until the physical channel associated with the transfer becomes available. Once the physical channel is available, the DMA transfer 406 may be performed. After the DMA transfer 406 completes, a bit in a channel interrupt pending register 408 is set to indicate the completion of the transfer. A new transfer may now occupy the physical channel associated with the completed transfer. The number of registers in the control registers 400 and the triggering registers 402 may vary depending on the specific DMA implementation. For example, the C6x1x family of DSP systems include four general registers and the MegaStar3 DSP system includes 14 general registers. Typically, at least a source and destination memory address, as well as a count value indicating the number of elements in each frame of the transfer blocks, is included in the control register 400.--

Rewrite paragraph [0031] as follows:

--[0031] Numerous optimal functions preferably exist in the asynchronous copy interface 212 for carrying out various transfer types. For example, a first function may be designed to handle 1D-to-2D 8-bit transfers and a second function may be designed to handle two-dimensional to two-dimensional (2D-to-2D) 8-bit transfers. The preferred process to determine the memory location of the optimal command function uses a vector table as described below.

Referring to Figure 5 and 6, an exemplary vector table is shown in accordance with the preferred embodiments. The vector table comprises a handle table 500 that preferably contains the logical handles requested by the instantiated algorithm 206. Although any number of handles may exist, three such handles 502, 504, and 506 are shown to facilitate discussion. The first handle 502 may represent a logical channel configured for a 1D-to1D 8-bit transfer, whereas the second handle 504 and the third handle 506 may represent a logical channel configured for a 1D-to-2D 16-bit and a 2D-2D 16-bit transfer, respectively. A pointer may associate the handle 504 and the handle 506 with the physical channel identifiers 508 and 512 (physical_chan_id) and other configuration setting 511 and 515 respectively. The physical channel identifiers 508 and 512 may uniquely identify a physical channel supported by the DMA controller ~~104~~ 108. Associated to the physical channel identifiers 508 and 514 are the configuration identifiers 510 and 514 (config_id), respectively. The configuration identifiers 510 and 514 are used to directly determine (*i.e.*, without a search) the location of the optimal command function. In addition, the configuration identifiers 510 and 514 may represent a specific transfer type, as previously discussed. The handle table 500 and the associated physical channel and configuration identifiers preferably are stored in non-volatile memory coupled to the DMA manager 214.--